IN THE CLAIMS:

Please replace claims 1, 6 and 11 with the following:

1. (Twice Amended) A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit changing the pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from a preceding stage clocked inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.

6. (Twice Amended) A delay circuit comprising:

an inverter circuit controlled by a clock signal to which a first pulse signal is supplied, said inverter circuit changing the pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from a preceding stage inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.

11. (Amended) A delay circuit applied to a synchronizing circuit comprising:

a first delay line which includes unit delay elements and transfers a forward pulse signal;

a second delay line which includes unit delay elements and transfers a backward pulse signal; and

a state holding section which is brought into a set state or a reset state according to a transfer position of the forward pulse signal transferred along said first delay line and said

backward pulse signal transferred along said second delay line in the set state and a clock signal along said second delay line in the reset state,

wherein each of said unit delay elements constituting said first and second delay lines includes:

a clocked inverter circuit to which a first pulse signal corresponding to one of said forward and backward pulse signals output from a preceding delay unit is supplied, said clocked inverter circuit changing a pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from a preceding stage clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.